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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,581	07/25/2001	Takahiro Ohnakado	401308	6065

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EXAMINER
RICHARDS, N DREW

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/911,581	Applicant(s) OHNAKADO, TAKAHIRO
	Examiner N. Drew Richards	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,13 and 16* is/are rejected.

7)☒ Claim(s) *7,8,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 5939753) in view of Chang et al. (U.S. Publication US 2002/0086467 A1).

Ma et al. disclose in figures 8 and 10, a substrate 11, a Si MOS transistor 115 and an ESD protection circuit 160 in high frequency devices. Ma et al. do not disclose the ESD circuit having m lateral polysilicon diodes on the substrate, each of the lateral polysilicon diode having a forward direction and a reverse direction, wherein m lateral polysilicon diode are connected is series in the forward direction between a high-frequency I/O signal line to an externally supplied voltage.

Chang et al. teach an ESD circuit. Chang et al. teach in figure 13B or 13C, an ESD circuit comprising m lateral polysilicon diodes on a substrate, the diodes having a forward direction and a reverse direction, wherein m lateral polysilicon diode are connected is series in the forward direction between a high-frequency I/O signal line to an externally supplied voltage. Chang et al. teach m being an integer greater than 1. In combination, the diode of Chang et al. would connect to a high-frequency I/O signal line of Ma et al.

With regard to the limitation of applying a reverse bias of less than 1.1 volts to each diode, this limitation is merely an intended use that does not structurally distinguish over the prior art.

Ma et al. and Chang et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form m lateral polysilicon diodes connected between the I/O signal line and Vdd as the ESD protection circuit. The motivation for doing so is the use of lateral polysilicon diodes provides faster ESD protection response as it is isolated from the substrate and has reduced parasistic substrate capacitance. Therefore, it would have been obvious to combine Ma et al. with Chang et al. to obtain the invention of claim 1.

With regard to claim 2, Ma et al. disclose in figures 8 and 10, a substrate 11, a Si MOS transistor 115 and an ESD protection circuit 160 in high frequency devices. Ma et al. do not disclose the ESD circuit having n lateral polysilicon diodes on the substrate, each of the lateral polysilicon diode having a forward direction and a reverse direction, wherein n lateral polysilicon diode are connected is series in the forward direction between ground GND and a high-frequency I/O signal.

Chang et al. teach an ESD circuit. Chang et al. teach in figure 13B or 13C, an ESD circuit comprising n lateral polysilicon diodes on a substrate, the diodes having a forward direction and a reverse direction, wherein m lateral polysilicon diode are connected is series in the forward direction between VSS and a high-frequency I/O

signal line. It is well known that VSS may commonly be grounded during device operation, thus Chang et al. is considered to have the diodes connected to ground. Chang et al. teach n being an integer greater than 1. In combination, the diode of Chang et al. would connect to a high-frequency I/O signal line of Ma et al.

With regard to the limitation of applying a reverse bias of less than 1.1 volts to each diode, this limitation is merely an intended use that does not structurally distinguish over the prior art.

Ma et al. and Chang et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form n lateral polysilicon diodes connected between ground and a high-frequency I/O signal line as the ESD protection circuit. The motivation for doing so is the use of lateral polysilicon diodes provides faster ESD protection response as it is isolated from the substrate and has reduced parasistic substrate capacitance. Therefore, it would have been obvious to combine Ma et al. with Wang to obtain the invention of claim 2.

With regard to claim 3, this claim is a combination of claims 1 and 2 in that it includes both m diodes connected between a signal line and VDD and n diodes connected between a ground and a signal line. Chang et al. teach both the set of m diodes and the set of n diodes and has been properly combined with Ma et al. above, thus Ma et al. with Chang et al. teach all the limitations of claim 3.

With regard to claim 4, in the combination of Ma et al. with Chang et al., no lateral polysilicon diode is connected to any signal line other than the high frequency I/O signal line as all the devices of Ma et al., and thus all signal lines, are considered high frequency devices.

3. Claims 5, 6, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 5939753) in view of Wang (U.S. Patent No. 6351363 B1).

With regard to claims 5 and 6, Ma et al. disclose in figures 8 and 10, a substrate 11, a Si MOS transistor 115 and an ESD protection circuit 160 in high frequency devices a a capacitor having lower and upper polysilicon electrodes and the transistor having a polysilicon gate. Ma et al. do not disclose the ESD circuit having a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, a high-frequency I/O signal line to an externally supplied voltage VDD.

Wang teaches an ESD circuit. Wang teaches in figure 3, an ESD circuit comprising a first lateral polysilicon diode 11 on a substrate, the diode having a forward direction and a reverse direction, wherein the diode connects, in the forward direction, a I/O signal line to an externally supplied voltage VDD. In combination, the diode of Wang would connect to a high-frequency I/O signal line of Ma et al.

Ma et al. teach the gate electrode being polysilicon and the first and second electrodes of the capacitor being polysilicon. Wang teach the diode being polysilicon. Ma et al. combined with Wang, the diode and lower electrode of the capacitor are from a first polysilicon layer and the upper electrode of the capacitor and the gate are from a second polysilicon layer. Whether formed simultaneously or in different steps, the limitation of the first lateral polysilicon diode and lower electrode of the capacitor being from a first polysilicon layer and the polysilicon gate being from a second polysilicon layer as claimed only structurally requires the device to have the capacitor electrodes, gate, and diode formed of polysilicon.

Ma et al. and Wang are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a lateral polysilicon diode connected between the I/O signal line and Vdd as the ESD protection circuit. The motivation for doing so is the use of lateral polysilicon diode provides faster ESD protection response as it is isolated from the substrate and has reduced parasistic substrate capacitance. Therefore, it would have been obvious to combine Ma et al. with Wang to obtain the invention of claims 5 and 6.

With regard to claim 13 and 16, Ma et al. disclose in figures 8 and 10, a substrate 11, a Si MOS transistor 115 and an ESD protection circuit 160 in high frequency devices a a capacitor having lower and upper polysilicon electrodes and the transistor having a polysilicon gate. Ma et al. do not disclose the ESD circuit having a first lateral

polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, ground to a high-frequency I/O signal line.

Wang teaches an ESD circuit. Wang teaches in figure 3, an ESD circuit comprising a first lateral polysilicon diode 11 on a substrate, the diode having a forward direction and a reverse direction, wherein the diode connects, in the forward direction, ground (VSS in figure 3, disclosed as ground on column 4 line 6) to an I/O signal line. In combination, the diode of Wang would connect to a high-frequency I/O signal line of Ma et al.

Ma et al. teach the gate electrode being polysilicon and the first and second electrodes of the capacitor being polysilicon. Wang teach the diode being polysilicon. Ma et al. combined with Wang, the diode and lower electrode of the capacitor are from a first polysilicon layer and the upper electrode of the capacitor and the gate are from a second polysilicon layer. Whether formed simultaneously or in different steps, the limitation of the first lateral polysilicon diode and lower electrode of the capacitor being from a first polysilicon layer and the polysilicon gate being from a second polysilicon layer as claimed only structurally requires the device to have the capacitor electrodes, gate, and diode formed of polysilicon.

Ma et al. and Wang are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a lateral polysilicon diode connected ground and the signal line as the ESD protection circuit. The motivation for doing so is the use of a

lateral polysilicon diode provides faster ESD protection response as it is isolated from the substrate and has reduced parasistic substrate capacitance. Therefore, it would have been obvious to combine Ma et al. with Wang to obtain the invention of claims 13 and 16.

Allowable Subject Matter

4. Claims 7, 8, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 5/20/03 have been fully considered but they are not persuasive.

6. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

7. With regard to claims 5 and 6 that the examiner has not explained how the teaching of Wang would produce the structure of claims 5 and 6 since Wang does not teach a capacitor and thus there can be no sharing of capacitor plates and transistor gates in common polysilicon layers. This argument is not persuasive. Claims 5 and 6 require the capacitor plates to be polysilicon, the transistor gate to be polysilicon, and

the lateral polysilicon diodes to be polysilicon. Claims 5 and 6 say that some of these layers are from the same "first" or "second" polysilicon layer. Ma et al. teach polysilicon used for the gate and capacitor plates. Wang teach polysilicon for the diodes. Thus, the diode, capacitor plates, and transistor gate are all formed from polysilicon. There is no structural difference in the device if the diode and first capacitor plate are formed of polysilicon deposited as one layer or whether two separate polysilicon layers are deposited for each structure. Being formed from a common polysilicon layer may include a different method than that of Ma et al. with Wang, but the final structure does not depend on the method of forming it. The final structure merely requires the diode and lower electrode of the capacitor are formed of polysilicon and that the upper electrode of the capacitor and the gate are formed of polysilicon. This final structure is taught by the combination of references and thus the rejection is considered proper.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (703) 306-5946. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NDR
July 25, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800